

# **JEDEC STANDARD**

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## **Standard for Description of 3.3 V NFET Bus Switch Devices**

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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## STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES

(From Board Ballot JCB-00-98, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

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### 1 Scope

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This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description.

The purpose of this document is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

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### 2 Definitions for the purpose of this document

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**switch device:** A semiconductor logic device designed to connect or disconnect busses or control signals without active drivers in the connection path.

**connect:** A state in a switch device characterized by a minimum series impedance through the designated electrical path.

**disconnect:** A state in a switch device characterized by the high series impedance of the designated electrical path.

### 3 Standard specifications

#### 3.1 Absolute maximum continuous ratings<sup>1,2</sup>

Symbol	Parameter	Rating	Units
V <sub>DD</sub>	Supply voltage	-0.5 to 4.6	V
V <sub>I</sub>	dc input voltage, control terminals <sup>(3)</sup>	-0.5 to 4.6	V
V <sub>SW</sub>	dc switch voltage <sup>(3)</sup>	-0.5 to 4.6	V
I <sub>IK</sub>	dc input clamp	-50	mA
I <sub>OK</sub>	dc clamp current, switch terminals	-50	mA
I <sub>SW</sub>	dc continuous channel current	120	mA
T <sub>STG</sub>	Storage temperature	-65 to 150	°C

NOTE 1 Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

NOTE 2 Under transient conditions these ratings may be exceeded as defined elsewhere in this specification.

NOTE 3 The dc negative voltage ratings may be exceeded if the dc input clamp current ratings are observed.

#### 3.2 Recommended operating conditions

Symbol	Parameter	Min	Max	Unit
V <sub>DD</sub>	Supply voltage	3.0	3.6	V
V <sub>IN</sub>	Control input voltage	0	3.6	V
V <sub>SW</sub>	Switch terminal voltage	0	3.6	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

#### 3.3 Capacitance<sup>(1)</sup>

Symbol	Parameter	Condition	Typ.	Unit
C <sub>IN</sub>	Control input capacitance			pF
C <sub>SW</sub>	Switch terminal capacitance	Switch disconnected		pF

NOTE 1 Capacitance is characterized but not tested

### 3 Standard specifications (cont'd)

#### 3.4 Power supply characteristics

Symbol	Description	Test Conditions	Max	Unit
$I_{DD}$	Quiescent power supply current	$V_{DD} = 3.6 \text{ V}$ $V_{SW} = \text{GND or } V_{DD}$		mA
$\Delta I_{DD}$	Quiescent power supply current TTL control inputs high <sup>(1)</sup>	$V_{DD} = 3.6 \text{ V}$ $V_{IN} = 2.0 \text{ V}$ $V_{SW} = \text{GND}$		$\mu\text{A}$
$Q_D$	Dynamic power supply current <sup>(2)</sup>	$V_{SW} = \text{GND}$ Control pin toggling at 10 MHz and 50% duty cycle		$\mu\text{A}/\text{MHz}$

NOTE 1 Per TTL driven control input

NOTE 2 All switch inputs grounded. One control pin toggling. All other control pins at  $V_{DD}$  or GND.

#### 3.5 Switching characteristics over operating range

Symbol	Description	Min	Typ	Max	Unit
$t_{PLH}$ $t_{PHL}$	Data path propagation delay <sup>(1,2)</sup>	—			ns
$t_{PZH}$ $t_{PZL}$	Switch connect delay <sup>(1)</sup>	—			ns
$t_{PHZ}$ $t_{PLZ}$	Switch disconnect delay <sup>(1)</sup>	—			ns

NOTE 1 Path must be specified.

NOTE 2 This parameter is not tested.

### 3 Standard specifications (cont'd)

#### 3.6 DC specifications

Symbol	Parameter	Test Conditions	Min	Max	Unit
$V_{IH}$	High-level input voltage		2.0	—	V
$V_{IL}$	Low-level input voltage		—	0.8	V
$V_{PASS}$	Pass voltage drop ( $V_{DD} - V_O$ )	$V_{SW} = V_{DD}$ $V_{DD} = \text{Note 5}$ $I_{out} = -100 \mu A$			V
$R_{ON}$	Switch connect resistance <sup>(2,3)</sup>	$V_{SW} = 0 \text{ V}$   $I_{SW} = (1)$	—		$\Omega$
		$V_{SW} = 2.4 \text{ V}$   $I_{SW} = (1)$	—		$\Omega$
$I_{OS}$	Short circuit current <sup>(2,4)</sup>	$V_{SW} = V_{DD}$ $V_{OUT} = \text{GND}$		—	mA
$I_{DD}$	Quiescent power supply current	$V_{DD} = \text{Max.}$ , $V_{IN} = V_{DD} \text{ or GND}$	—		$\mu A$
$V_{IK}$	Clamp diode voltage	Switch Terminals $I_{SW} = -18 \text{ mA}$	—		V
		Control Terminals, $I_{IN} = -18 \text{ mA}$	—		V
$I_{OZ}$	Current during switch disconnect	$V_{DD} = \text{Max.}$ $V_{SW} = \text{GND to } 3.6 \text{ V}$ $V_{OUT} = \text{GND}$	—		$\mu A$
$I_{IL}$ $I_{IH}$	Control input current	$V_{DD} = \text{Max.}$   $V_I = \text{GND}$ $V_I = V_{DD}$	—		$\mu A$
$I_{OFF}$	Switch terminal leakage <sup>(6)</sup>	$V_{DD} = 0 \text{ V}$ $V_{SW} = 3.6 \text{ V}$	—		$\mu A$

NOTE 1 See the manufacturer's data sheet.

NOTE 2 The connect path must be specified.

NOTE 3 Resistance is measured as  $\Delta V / \Delta I$ . For  $V_{SW} = 0 \text{ V}$ , the resistance is measured while  $V_{OUT}$  is pulled higher to the designated current level. For  $V_{SW} = 2.4 \text{ V}$ , the resistance is measured while  $V_{OUT}$  is pulled lower to the designated current level.

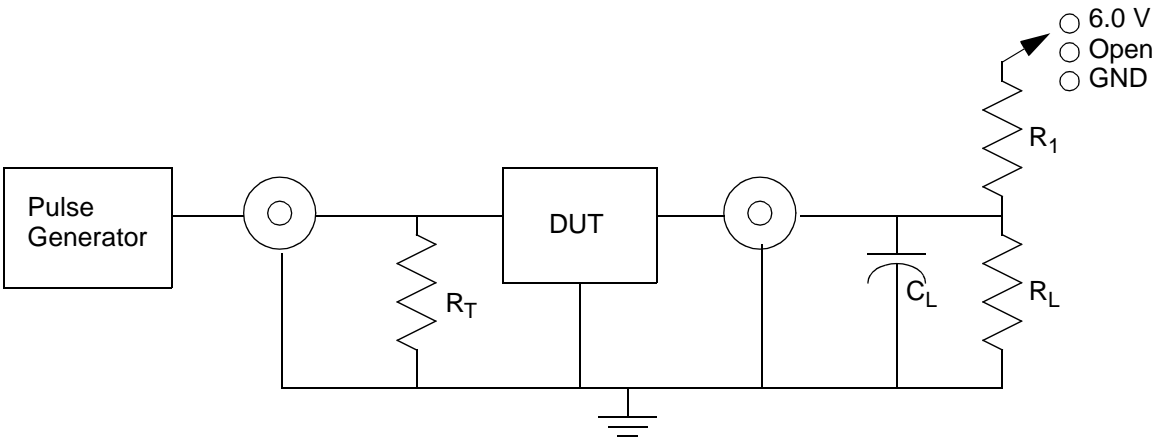
NOTE 4 Not more than one output should be tested at a time. Duration of the test must not exceed one second. This is an optional parameter.

NOTE 5 Optional specification for voltage translation.  $V_{DD}$  = the recommended voltage for 3.3 V to 2.5 V voltage translation. This parameter is characterized but not tested.

NOTE 6 This is an optional parameter.



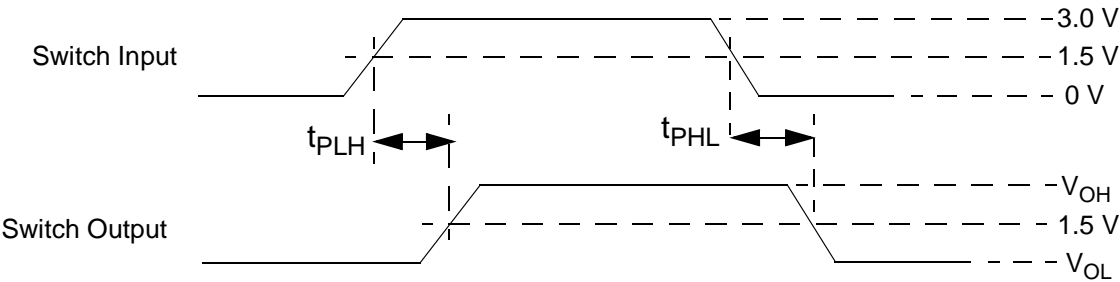
4 Test circuits and switching waveforms



$C_L = 50 \text{ pF}$  or equivalent (includes test setup and probe capacitance).  
 $R_L = R_1 = 500 \text{ } \Omega$  or equivalent  
 $R_T$  = Pulse generator termination resistance  
Pulse generator has the following characteristics:  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ ,  $\text{PRR} \leq 10 \text{ MHz}$

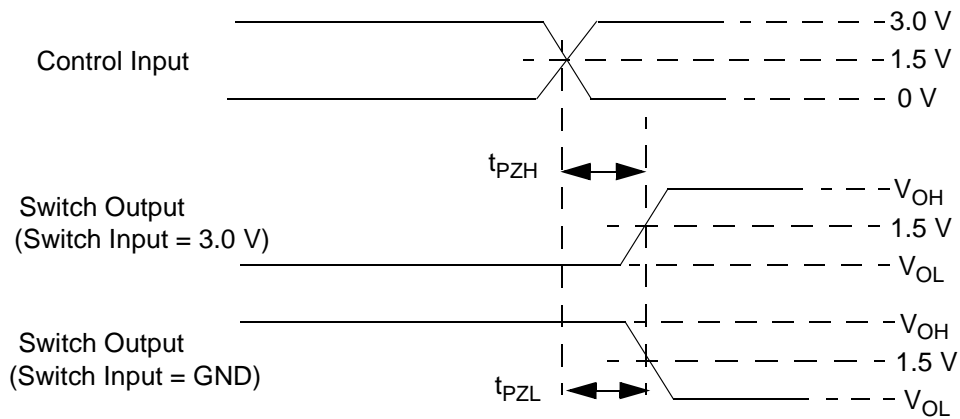
Test	Switch S1
$t_{PLH}$	Open
$t_{PHL}$	Open
$t_{PZH}$	Open
$t_{PZL}$	6.0 V
$t_{PHZ}$	Open
$t_{PLZ}$	6.0 V

4.1 Propagation delay measurements

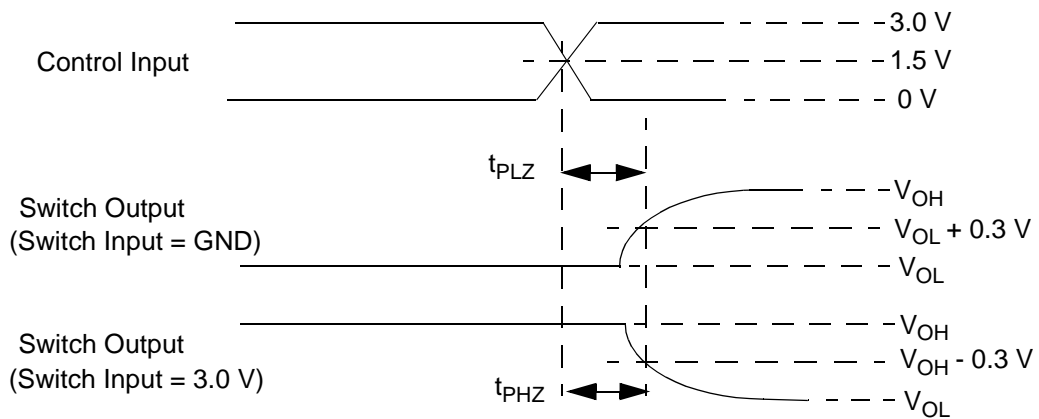


## 4 Test circuits and switching waveforms (cont'd)

### 4.2 Connect delay measurements



### 4.3 Disconnect delay measurements



NOTE Reference to Other Applicable JEDEC Standards and Publications



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